IN THE CLAIMS

Please amend the claims to read as follows:

Listing of Claims

Claims 1-10 (Cancelled).

11. (Currently Amended) An input control apparatus comprising:

a receiving section that receives a signal including bits of a systematic part and bits of parity parts comprising a plurality of sequences, the signal being generated in an external transmission apparatus by turbo coding and puncturing information;

a rate dematching processing section that performs rate dematching processing on the received signal; and

a bit number reduction section that discards bits from the systematic part and bits from the parity parts ~~comprising the plurality of sequences~~ so that the number of bits in each ~~one~~ sequence of the parity parts is less than the number of bits in the systematic part, at a timing between the rate dematching processing and ~~before performing~~ turbo decoding on the signal subjected to the rate dematching processing.

12. (Currently Amended) An input control apparatus comprising:

a receiving section that receives a signal including bits of a systematic part and bits of parity parts comprising a plurality of sequences, the signal being generated in an external transmission apparatus by turbo coding and puncturing information;

a rate dematching processing section that performs rate dematching processing on the received signal; and

a bit number reduction section that discards bits from the systematic part and bits from the parity parts so that the number of bits in each sequence of the parity parts is less than the number of bits in the systematic part, before performing turbo decoding on the signal subjected to the rate dematching processing, wherein

~~The input control apparatus according to claim 11, wherein~~ the bit number reduction section discards the bits from the systematic part and the bits from the parity parts ~~comprising the plurality of sequences~~ so that the number of bits in the parity parts is determined in accordance with a coding rate and/or coding block length of a bit sequence received as input in a turbo decoder.

13. (Currently Amended) The input control apparatus according to claim 12, wherein the bit number reduction section discards the bits from the systematic part and the bits from the parity parts ~~comprising the plurality of sequences~~ so that the number of bits in the parity parts decreases as the coding rate of the bit sequence received as input in the turbo decoder decreases and the number of bits in the parity parts increases as the coding rate increases.

14. (Currently Amended) The input control apparatus according to claim 12, wherein the bit number reduction section discards the bits from the systematic part and the bits from the parity parts ~~comprising the plurality of sequences~~ so that the number of bits in the parity parts decreases as the coding block length received as input in the turbo decoder increases and the

number of bits in the parity parts increases as the coding block length decreases.

15. (Currently Amended) An input control method comprising the steps of:

receiving a signal including bits of a systematic part and bits of parity parts comprising a plurality of sequences, the signal being generated in an external transmission apparatus by turbo coding and puncturing information;

performing rate dematching processing on the received signal; and

discarding bits from the systematic part and bits from the parity parts ~~comprising the plurality of sequences~~ so that the number of bits in each ~~one~~ sequence of the parity parts is less than the number of bits in the systematic part, at a timing between the rate dematching processing and ~~before performing~~ turbo decoding on the signal subjected to the rate dematching processing.

16. (New) An input control method comprising the steps of:

receiving a signal including bits of a systematic part and bits of parity parts comprising a plurality of sequences, the signal being generated in an external transmission apparatus by turbo coding and puncturing information;

performing rate dematching processing on the received signal; and

discarding bits from the systematic part and bits from the parity parts so that the number of bits in each sequence of the parity parts is less than the number of bits in the systematic part, before performing turbo decoding on the signal subjected to the rate dematching processing, wherein

in the discarding, the bits from the systematic part and the bits from the parity parts are discarded so that the number of bits in the parity parts is determined in accordance with a coding rate and/or coding block length of a bit sequence received as input in a turbo decoder.